

IN THE CLAIMS

✓ Please cancel claims 9, 10, 14, 18 and 33 without prejudice or disclaimer, and amend claims 1, 4, 11 thru 13, 15 thru 17, 19, 20, 25, 26, 28 and 34 thru 40, as follows:

1 1. (Currently Amended) An apparatus, comprising:

2 a converter for converting an input optical signal to an original electrical signal;

3 an identification unit for receiving said original electrical signal, for generating a

4 first signal corresponding to comprising said original electrical signal delayed by a

5 pretermine~~d~~ predetermine quantity of time, for generating a second signal corresponding

6 to comprising said original electrical signal not delayed, for comparing said first and

7 second signals, for forming a third signal in dependence upon said comparing of said first

8 and second signals, and for detecting a bit rate in dependence upon said third signal;

9 a clock generator for generating a separate reference clock signal in dependence

10 upon said detected bit rate; and

11 a recovery unit for recovering an input clock signal and data from said input

12 optical signal in dependence upon said reference clock signal, and;

13 wherein said identification unit further comprises:

14 a first unit for delaying said original electrical signal, for performing [[said]] an

15 exclusive -OR operation upon said first and second signals, and for forming said third

16 signal in dependence upon said exclusive-OR operation performed upon said first and

17 second signals; and

18           a second unit for filtering said third signal, and for detecting said bit rate in  
19           dependence upon a voltage level of said filtered third signal;

20           said second unit comprising:

21           a filter for filtering said third signal;

22           an analog-to-digital converter for receiving said filtered third signal, and  
23           for converting said filtered third signal from an analog signal to a digital signal;  
24           and

25           a bit rate deriving unit for deriving said bit rate in dependence upon  
26           information related to a voltage level of said digital signal received from said  
27           analog-to-digital converter and a predetermined bit rate.

28           2. (Original) The apparatus of claim 1, said apparatus corresponding to an optical  
29           receiver receiving optical signals having a plurality of different bit rates.

1           3. (Original) The apparatus of claim 1, said bit rate of said input optical signal  
2           corresponding to a transmission rate.

1           4. (Currently Amended) The apparatus of claim 1, further comprising an  
2           amplifier for amplifying said original electrical signal received from said converter.

1           5. (Original) The apparatus of claim 4, said amplifier outputting said amplified

2 electrical signal to said identification unit.

1 6. (Original) The apparatus of claim 1, said converter corresponding to an  
2 optoelectric converter.

1 7. (Original) The apparatus of claim 1, said identification unit corresponding to a  
2 bit rate identification unit.

1 8. (Original) The apparatus of claim 1, said comparing performed by said  
2 identification unit corresponding to said identification unit performing an exclusive-OR  
3 logic operation upon said first and second signals.

Claims 9 and 10. (Cancelled)

1 11. (Currently Amended) The apparatus of claim [[10]] 1, said filtering  
2 corresponding to low-pass filtering.

1 12. (Currently Amended) The apparatus of claim [[10]] 1, said first unit  
2 corresponding to a bit rate identification signal generator.

1 13. (Currently Amended) The apparatus of claim [[10]] 1, said second unit

2 corresponding to a bit rate deriving unit.

Claim 14. (Cancelled)

1 15. (Currently Amended) The apparatus of claim [[10]] 1, said first unit  
2 comprising:

3 a buffer unit for receiving said original electrical signal, and for outputting two  
4 duplicate signals substantially equivalent to said original electrical signal, said two  
5 duplicate signals corresponding to comprising a primary signal and a secondary signal;

6 a delay unit for receiving said primary signal, for delaying said primary signal by  
7 said predetermined quantity of time, and for outputting said delayed primary signal, said  
8 delayed primary signal corresponding to said first signal and said secondary signal  
9 corresponding to said second signal; and

10 an operator unit for performing said exclusive-OR logic operation upon said first  
11 and second signals.

1 16. (Currently Amended) The apparatus of claim 1, said clock generator  
2 comprising a plurality of oscillators for generating clocking signals of different  
3 frequencies, and selectively operating said oscillators being selectively operated to  
4 generate said reference clock signal in dependence upon said bit rate detected by said  
5 identification unit.

1           17. (Currently Amended) A method of operating a receiver which functions  
2           independently of a bit rate of a received signal, comprising:  
3           receiving an original signal;  
4           generating a resultant signal by comparing performing an exclusive-OR operation  
5           on a first signal and a second signal, said first signal corresponding to said original signal  
6           delayed by a predetermined quantity of time, said second signal corresponding to said  
7           original signal not delayed;  
8           determining a bit rate of said original signal in dependence upon by low-pass  
9           filtering said resultant signal, and determining a voltage level of the low-pass filtered  
10           resultant signal;  
11           generating a reference clock signal separate from said original signal and in  
12           dependence upon said determined bit rate; and  
13           recovering an input clock signal and data from said original signal in dependence  
14           upon said reference clock signal.

11           Claim 18. (Cancelled)

1           19. (Currently Amended) The method of claim [[18]] 17, said original signal  
2           comprising an input optical signal, said method, further comprising:  
3           said original signal corresponding to an input optical signal;

4                   converting said input optical signal to an electrical signal;

5                   outputting two duplicate signals substantially equivalent to said electrical signal,

6                   said two duplicate signals ~~corresponding to~~ comprising a primary signal and a secondary

7                   signal; and

8                   delaying said primary signal by said predetermined quantity of time, and

9                   outputting said primary signal, said delayed primary signal ~~corresponding to~~ comprising

10                  said first signal.

1                  20. (Currently Amended) The method of claim 17, said first[[,]] and second, ~~and~~

2                  third signals ~~corresponding to~~ comprising electrical signals.

1                  21. (Original) The method of claim 17, said method corresponding to receiving

2                  signals having a plurality of different bit rates.

1                  22. (Original) The method of claim 17, said original signal received

2                  corresponding to a plurality of original signals received, said recovering of said input

3                  clock signal and data from said original signal being performed for said plurality of

4                  original signals received, said plurality of original signals received having a respective

5                  plurality of different bit rates.

1                  23. (Original) The method of claim 17, said recovering of said input clock signal

2 and data from said original signal being performed for a plurality of original signals  
3 received, said plurality of original signals received having a respective plurality of  
4 different bit rates.

1 24. (Original) The method of claim 17, said method corresponding to receiving  
2 optical signals having a plurality of different bit rates.

1 25. (Currently Amended) The method of claim 17, further comprising:  
2 receiving an input optical signal;  
3 converting said input optical signal to an original electrical signal;  
4 outputting two duplicate signals substantially equivalent to said original electrical  
5 signal, said two duplicate signals ~~corresponding to~~ comprising a primary signal and a  
6 secondary signal; and  
7 delaying said primary signal by said predetermined quantity of time, and  
8 outputting said primary signal, said delayed primary signal ~~corresponding to~~ comprising  
9 said first signal, said outputted primary signal comprising said second signal.

1 26. (Currently Amended) The method of claim 17, said receiving of said original  
2 signal being performed by an optoelectric converter, said original signal being an optic  
3 signal, said optoelectric converter converting said original optic signal to an electrical  
4 signal, said method further comprising:

5           said receiving of said original signal being performed by an optoelectric converter,  
6    said original signal being an optic signal, said optoelectric converter converting said  
7    original optic signal to an electrical signal;

8           outputting two duplicate signals substantially equivalent to said electrical signal,  
9    said two duplicate signals corresponding to comprising a primary signal and a secondary  
10   signal, said outputting of said two duplicate signals being performed by a buffer; and

11           delaying said primary signal by said predetermined quantity of time, and  
12    outputting said primary signal, said delayed primary signal corresponding to comprising  
13   said first signal, and said outputted primary signal comprising said second signal.

1           27. (Original) The method of claim 17, said generating of said reference clock  
2    signal being performed by a clock generator, said clock generator comprising a plurality  
3    of oscillators generating clocking signals of different frequencies and selectively  
4    operating said oscillators to generate said reference clock signal in dependence upon said  
5    detected bit rate.

1           28. (Currently Amended) An apparatus, comprising:  
2           a converter for converting an input optical signal to an original electrical signal;  
3           an identification unit for receiving said original electrical signal, for generating a  
4    first signal corresponding to comprising said original electrical signal delayed by a  
5    preetermined predetermined quantity of time, for generating a second signal corresponding

6        to comprising said original electrical signal not delayed, for forming a third signal by  
7        performing an exclusive-OR logic operation upon said first and second signals, and for  
8        detecting a bit rate in dependence upon said third signal;

9                a clock generator for generating a reference clock signal in dependence upon said  
10        detected bit rate; and

11                a recovery unit for recovering an input clock signal and data from said input  
12        optical signal in dependence upon said reference clock signal;

13        said identification unit comprising:

14                a first unit for delaying said original electrical signal, for performing said  
15        exclusive-OR operation upon said first and second signals, and for forming said third  
16        signal; and

17                a second unit for filtering said third signal, and for detecting said bit rate in  
18        dependence upon a voltage level of said filtered third signal.

1                29. (Original) The apparatus of claim 28, said clock generator comprising a  
2        plurality of oscillators generating clocking signals of different frequencies and  
3        selectively operating said oscillators to generate said reference clock signal in  
4        dependence upon said bit rate detected by said identification unit.

1                30. (Original) The apparatus of claim 28, said input optical signal corresponding  
2        to a plurality of input optical signals, said recovering of said input clock signal and data

3       from said input optical signal being performed for each of said plurality of input optical  
4       signals, said plurality of input optical signals received having a plurality of different bit  
5       rates.

1           31. (Original) The apparatus of claim 30, said converter corresponding to an  
2       optoelectric converter.

1           32. (Original) The apparatus of claim 31, said identification unit corresponding  
2       to a bit rate identification unit.

Claim 33. (Cancelled)

1           34. (Currently Amended) The apparatus of claim [[33]] 28, said second unit  
2       comprising:

3           a filter for filtering said third signal;  
4           an analog-to-digital converter for receiving said filtered third signal, and for  
5       converting said filtered third signal from an analog signal to a digital signal; and  
6           a determiner for determining said bit rate in dependence upon said digital signal  
7       received from said analog-to-digital converter.

1           35. (Currently Amended) The apparatus of claim [[33]] 28, said first unit

2 comprising:

3 a buffer unit for receiving said original electrical signal, and for outputting two  
4 duplicate signals substantially equivalent to said original electrical signal, said two  
5 duplicate signals corresponding to comprising a primary signal and a secondary signal;

6 a delay unit for receiving said primary signal, for delaying said primary signal by  
7 said predetermined quantity of time, and for outputting said primary signal, said delayed  
8 primary signal corresponding to comprising said first signal; and

9 an operator unit for performing said exclusive-OR logic operation upon said first  
10 and second signals.

1 36. (Currently Amended) The apparatus of claim [[33]] 28, said clock generator  
2 comprising a plurality of oscillators for generating clocking signals of different  
3 frequencies, and selectively operating said oscillators being selectively operated to  
4 generate said reference clock signal in dependence upon said bit rate detected by said  
5 identification unit.

1 37. (Currently Amended) The apparatus of claim [[33]] 28, said filtering  
2 corresponding to low-pass filtering.

1 38. (Currently Amended) The apparatus of claim 37, said second unit comprising:  
2 a filter for filtering said third signal;

3                   an analog-to-digital converter for receiving said filtered third signal, and for  
4                   converting said filtered third signal from an analog signal to a digital signal; and  
5                   a determiner for determining said bit rate in dependence upon said digital signal  
6                   received from said analog-to-digital converter.

1                   39. (Currently Amended) The apparatus of claim 38, said first unit comprising:

2                   a buffer unit for receiving said original electrical signal, for outputting two  
3                   duplicate signals substantially equivalent to said original electrical signal, said two  
4                   duplicate signals corresponding to comprising a primary signal and a secondary signal;  
5                   a delay unit for receiving said primary signal, for delaying said primary signal by  
6                   said predetermined quantity of time, and for outputting said primary signal, said delayed  
7                   primary signal corresponding to comprising said first signal; and  
8                   an operator unit for performing said exclusive-OR logic operation upon said first  
9                   and second signals.

1                   40. (Currently Amended) The apparatus of claim 39, said clock generator  
2                   comprising a plurality of oscillators for generating clocking signals of different  
3                   frequencies, and selectively operating said oscillators being selectively operated to  
4                   generate said reference clock signal in dependence upon said bit rate detected by said  
5                   identification unit.